UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/613,494	07/01/2003	Jun-Young Lee	50391/DBP/Y35	4433

23363 7590 02/08/2006

CHRISTIE, PARKER & HALE, LLP
PO BOX 7068
PASADENA, CA 91109-7068

EXAMINER	
MOON, SEOKYUN	
ART UNIT	PAPER NUMBER
2675	

DATE MAILED: 02/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/613,494	LEE, JUN-YOUNG	
	Examiner	Art Unit	
	Seokyun Moon	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-7 and 9-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-7 and 9-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/01/03 & 2/02/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 1**, **2**, **6**, **7**, **9**, **10**, **14**, **15**, and **16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Onozawa et al. (U.S. Pub. No. 2002/0175883 A1, herein after referred to as "Onozawa").

As to **claim 1**, Onozawa teaches an apparatus for driving a plasma display panel ("*plasma display apparatus*"), which has a panel capacitor (It is inherent to include a capacitor in the drawing of a plasma display panel to indicate or to show the functional responses of X and Y electrodes as a capacitive load for a sustain discharge in the apparatus for driving a plasma display panel: [*Appl. No. 10/613,494 pg 2 lines 10-12*] herein after, it is referred to as "E capacitor") [*fig. 1* and *3C*], the apparatus comprising:

a first switch ("*Q22*") and a second switch ("*SW1*") being coupled in series between a first power source ("*-Vs2*") for supplying a first voltage and a terminal that goes to a sustain electrode.

a third switch ("*Q21*") and a fourth switch ("*SW3*") being coupled in series between the terminal that goes to the sustain electrode and a second power source (Vs1) for supplying a second voltage;

a first capacitor ("*C*") coupled between a common contact between the first switch and the second switch and a common contact between the third switch and the fourth switch; and

a fifth switch ("*SW2*") coupled between the first capacitor and a third power source ("*+Vw*") supplying a third voltage [*fig. 3C*] [*par. (0017)*].

Onozawa fails to teach expressly that the third voltage is substantially a middle voltage between the first voltage and the second voltage.

However, Onozawa does not provide any limitation on the range for the third voltage ("*Vw*") value except for that the voltage ("*Vs1 + (-Vs2) + Vw*") applied in the reset period or in the address period is greater than the sustain voltage ("*Vs1 + (-Vs2)*") [*par. (0012)*].

In addition, since applicant has not disclosed that assigning the third voltage to be a middle voltage value provides an advantage, is used for a particular purpose, or solves a stated problem, setting the 3rd voltage to be a middle voltage is an obvious matter of design choice.

Furthermore, given that Onozawa does not limit the range of the 3rd voltage, it would have been obvious to set the 3rd voltage to be a middle voltage between the 1st voltage and the 2nd voltage to simplify the required calculation regard to the driving voltages.

As to **claim 2**, Onozawa teaches the fifth switch ("*SW2*") is turned on so that the first capacitor ("*C*") is charged to a difference between the first voltage ("*-Vs2*") and the third voltage ("*+Vw*") [*fig. 3C*].

As to **claim 6**, Onozawa does not teach expressly a sixth, seventh, eighth, ninth, tenth switch, and a second capacitor.

However, it is inherent to include another electronic structure equivalent to the structure shown in [*fig. 3C*], in PDP driving circuit for another electrode.

Therefore, all of the claim limitations have already been discussed with respect to the rejection of claim 1.

As to **claim 7**, Onozawa teaches an apparatus for driving a plasma display panel, which has a panel capacitor ("*E capacitor*"), the apparatus comprising:

a first switch ("*Q22*") and a second switch ("*SW1*") being coupled in series between a first power source ("*-Vs2*") supplying a first voltage and a first terminal of the panel capacitor;

a third switch ("*Q21*") and a fourth switch ("*SW3*") being coupled in series between the first terminal of the panel capacitor and a second power source ("*Vs1*") supplying a second voltage;

a first signal line coupled to a common contact between the first switch and the second switch; and

a second signal line coupled to a common contact between the third switch and the fourth switch,

wherein a voltage between the first signal line and the second signal line is a third voltage ("*+Vw*"), and the first voltage ("*-Vs2*") and the second voltage ("*Vs1*") are alternatively applied to the first terminal of the panel capacitor ("*E capacitor*") [*fig. 3C*].

Onozawa fails to teach expressly that the third voltage is substantially a middle voltage between the first voltage and the second voltage.

However, Onozawa does not provide any limitation on the range for the third voltage ("*Vw*") value except for that the voltage ("*Vs1 + (-Vs2) + Vw*") applied in the reset period or in the address period is greater than the sustain voltage ("*Vs1 + (-Vs2)*") [*par. (0012)*].

In addition, since applicant has not disclosed that assigning the third voltage to be a middle voltage value provides an advantage, is used for particular purpose, or solves a stated problem, setting the 3rd voltage to be a middle voltage is an obvious matter of design choice.

Furthermore, given that Onozawa does not limit the range of the 3rd voltage, it would have been obvious to set the 3rd voltage to be a middle voltage between the 1st voltage and the 2nd voltage to simplify the calculation regard to the driving voltages.

As to **claim 9**, Onozawa teaches a capacitor ("*C*") coupled between the first signal line and the second signal line and charged to the third voltage ("*+Vw*") [*fig. 3C*].

As to **claim 10**, Onozawa teaches the fifth switch ("*SW2*") coupled between a third power source (+Vw) supplying a voltage substantially corresponding to a summation of the second voltage and the third voltage, the fifth switch being turned on thereby charging the capacitor ("*C*") to the third voltage in the on state of the fourth switch ("*SW3*") [*fig. 3C*].

As to **claim 14**, Onozawa does not teach expressly a sixth, seventh, eighth, ninth, tenth switch, and a second capacitor.

However, it is inherent to include another electronic structure equivalent to the structure shown in [*fig. 3C*] in the PDP driving circuit for another electrode.

Onozawa teaches the apparatus comprising [*fig. 3C*]:

a fifth switch ("*Q22*") and a sixth switch ("*SW1*") being coupled in series between the first power source ("*-Vs2*") and a second terminal of the panel capacitor ("*E capacitor*");

a seventh switch ("*Q21*") and an eighth switch ("*SW3*") being coupled in series between the second terminal of the panel capacitor ("*E capacitor*") and the second power source ("*Vs1*");

a third signal line coupled to a common contact between the fifth switch and the sixth switch; and

a fourth signal line coupled to a common contact between the seventh switch and the eighth switch,

wherein a voltage between the third signal line and the fourth signal line is the third voltage, and the second voltage is applied to the second terminal of the panel capacitor while the first voltage is applied to the first terminal of the panel capacitor, and the first voltage is applied to the second terminal of the panel capacitor while the second voltage is applied to the first terminal of the panel capacitor .

As to **claim 15**, Onozawa teaches a method for driving a plasma display panel, in which the plasma display panel is driven by alternatively applying a first voltage ("*-Vs2*") and a second voltage ("*Vs1*") through a first signal line and a second signal line coupled to a first terminal of a panel capacitor [*fig. 3C*], the method comprising:

(a) applying a third voltage ("*+Vw*") between a common contact between a first switch ("*Q22*") and a second switch ("*SW1*") formed on the first signal line and a common contact between a third switch ("*Q21*") and a fourth switch ("*SW3*") formed on the second signal line, while the first voltage is applied to the first terminal of the panel capacitor by turning on the first switch and the second switch; and

(b) applying the third voltage between the common contact between the first switch and the second switch and the common contact between the third switch and the fourth switch, while the second voltage is applied to the first terminal of the panel capacitor by turning on the third switch and the fourth switch.

Onozawa fails to teach expressly that the third voltage is substantially a middle voltage between the first voltage and the second voltage.

However, Onozawa does not provide any limitation on the range for the third voltage ("*Vw*") value except for that the voltage ("*Vs1 + (-Vs2) + Vw*") applied in the reset period or in the address period is greater than the sustain voltage ("*Vs1 + (-Vs2)*") [*par. (0012)*].

In addition, since applicant has not disclosed that assigning the third voltage to be a middle voltage value provides an advantage, is used for particular purpose, or solves a stated problem, setting the 3rd voltage to be a middle voltage is an obvious matter of design choice.

Furthermore, given that Onozawa does not limit the range of the 3rd voltage, it would have been obvious to set the 3rd voltage to be a middle voltage between the 1st voltage and the 2nd voltage to simplify the calculation regard to driving voltages.

As to **claim 16**, Onozawa teaches the method applying the third voltage ("*+Vw*") between the common contact between the first switch ("*Q22*") and the second switch ("*SW1*") and the common contact between the third switch ("*Q21*") and the fourth switch ("*SW3*"), while the second voltage ("*Vs1*") is applied to the first terminal of the panel capacitor by turning on the third switch and the fourth switch, includes charging the third voltage to a capacitor ("*C*") coupled between the contact of the first switch, the contact of the second switch, the contact of the third switch and the contact of the fourth switch [*fig. 3C*].

3. **Claims 4**, **11**, **12**, **17**, and **18** rejected under 35 U.S.C. 103(a) as being unpatentable over Onozawa et al. in view of Ohba et al. (U.S. Pat. No. 5,670,974, herein after referred to as "Ohba").

As to **claim 4**, Onozawa fails to teach the apparatus comprising at least one inductor, a sixth switch, and a seventh switch.

However, Ohba teaches the apparatus ("*plasma display panel driver circuit*") comprising:

at least one inductor ("*34*") coupled to the first terminal of the panel capacitor ("*40*"); and

a sixth switch ("*30*" + "*31*") and a seventh switch ("*32*" and "*33*") being coupled in parallel between the inductor and the third power source ("*(1/2)Vs*" + "*28*").

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include the part comprising *FET switches 30, 32, diodes 31, 33,*

and *capacitor 29* of the *plasma display panel driver circuit* of Ohba, in Onozawa to reduce the power consumption in display driving circuit [Ohba: *col. 2 lines 47-49*].

As to **claim 11**, Onozawa fails to teach the apparatus comprising a power recovery section including at least one inductor.

However, Ohba teaches the apparatus ("*plasma display panel driver circuit*") comprising a power recovery section (the part comprising *FET switches 30, 32*, *diodes 31, 33*, and *capacitor 29* of the *plasma display panel driver circuit* shown in *fig. 3*) including at least one inductor ("*34*") coupled to the first terminal of the panel capacitor ("*40*"), the power recovery section changing a terminal voltage of the panel capacitor using a resonance generated between the inductor and the panel capacitor [*fig. 3*].

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include Ohba's power recovery section in Onozawa to reduce the power consumption in display driving circuit [Ohba: *col. 2 lines 47-49*].

As to **claim 12**, the combined device of Onozawa and Ohba teaches the power recovery section (the part comprising *FET switches 30, 32*, *diodes 31, 33*, and *capacitor 29* of the *plasma display panel driver circuit* shown in *fig. 3*) including a fifth switch ("*30*" + "*31*") and a sixth switch ("*32*" + "*33*") being coupled in parallel between the inductor ("*34*") and a third power source [*fig. 3*].

The combined device fails to teach expressly the voltage from the third power source to be the middle voltage corresponding to a difference of the first voltage and the second voltage.

However, the combined device does not provide any limitation on the range for the third voltage value except for that the voltage applied in the reset period or in the address period is greater than the sustain voltage [Onozawa: *par. (0012)]*.

In addition, since applicant has not disclosed that assigning the third voltage to be a middle voltage value provides an advantage, is used for particular purpose, or solves a stated problem, setting the 3rd voltage to be a middle voltage is an obvious matter of design choice.

Furthermore, given that Onozawa does not limit the range of the 3rd voltage, it would have been obvious to set the 3rd voltage to be a middle voltage between the 1st voltage and the 2nd voltage to simplify the calculation regard to the driving voltages.

As to **claim 17**, the combined apparatus of Onozawa and Ohba teaches the method comprising:

applying a third voltage (Onozawa: "*+Vw*") between a common contact between a first switch (Onozawa: "*Q22*") and a second switch (Onozawa: "*SW1*") formed on the first signal line and common contact between a third switch (Onozawa: "*Q21*") and a fourth switch (Onozawa: "*SW3*") formed on the second signal line, while the first voltage (Onozawa: "*-Vs2*") is applied to the first terminal of the panel capacitor by turning on the first switch and the second switch, further includes raising the voltage of the first terminal of the panel capacitor to the first voltage using a first resonance generated between an inductor (Ohba: "*81*") coupled to the first terminal of the panel capacitor (Ohba: "*82*") and the panel capacitor, and

applying the third voltage between the common contact between the first switch and the second switch and the common contact between the third switch and the fourth switch, while the second voltage (Onozawa: "*Vs1*") is applied to the first terminal of the panel capacitor by turning on the third switch and the fourth switch, further includes dropping the voltage of the first terminal of the panel capacitor to the second voltage using a second resonance generated between the inductor and the panel capacitor, before the second voltage is applied to the panel capacitor.

As to **claim 18**, the combined apparatus of Onozawa and Ohba teaches the method comprising:

applying a third voltage (Onozawa: "*+Vw*") between a common contact between a first switch (Onozawa: "*Q22*") and a second switch (Onozawa: "*SW1*") formed on the first signal line and a common contact between a third switch (Onozawa: "*Q21*") and a fourth switch (Onozawa: "*SW3*") formed on the second signal line, while the first voltage (Onozawa: "*-Vs2*") is applied to the first terminal of the panel capacitor by turning on the first switch and the second switch, further includes injecting current in the inductor through a path of a power source supplying the third voltage, the inductor, and the second signal line, before the first resonance is generated, and

applying the third voltage between the common contact between the first switch and the second switch and the common contact between the third switch and the fourth switch, while the second voltage (Onozawa: "*Vs1*") is applied to the first terminal to the panel capacitor by turning on the third switch and the fourth switch, further includes

injecting current in the inductor through a path of the first signal line, the inductor, and the power source, before the second resonance is generated.

4. **Claims 5** and **13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Onozawa in view of Kang (U.S. Pub. No. 2002/0033675 A1, herein after referred to as "Kang").

Onozawa fails to teach the first switch, the second switch, the third switch, and the fourth switch each have a body diode.

Kang teaches MOSFETs as the switches ("*Q1*", "*Q2*", "*Q3*", ...) used in the device for driving a plasma display panel [*fig. 14*].

It would have been obvious to one of ordinary skill in the art at the time of the invention to replace Onozawa's switches with MOSFETs as taught by Kang, to utilize additional factor such as voltage to control the switches in the driving circuits for PDPs.

Furthermore, examiner takes official notice that it is well known that body diodes exist between the drain and the source of each MOSFET due to the structure of diffusion layers.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include body diodes in the switches of the combination device of Onozawa and Kang to observe the functional behaviors or characteristics of MOSFET switches when the switches of Onozawa is replaced by Kang's MOSFETs.

Response to Arguments

5. Examiner made a new ground rejection with respect to claims 1-2, 4-7, and 9-18.

Examiner uses Onozawa (U.S. Pub. No. 2002/0175883 A1) and Ohba (U.S. Pat. No. 5,670,974), of which the U.S. filing dates would constitute 103 (a) references, to reject claims 1, 2, 4, 6, 7, 9, 10, 11, 12, 14, 15, 16, 17, and 18.

Therefore, all the references used for this Office action would be proper/valid references for 103 (a) rejections.

6. Applicant's arguments filed with respect to "*where the third voltage is substantially a middle voltage between the first voltage and the second voltage*" have been fully considered but they are not persuasive.

The applicant fails to provide specific voltage values or ranges for the first, second, and third voltages. Furthermore, Onozawa does not provide the limitation on the voltage levels to be accomplished by $Vs1$, $-Vs2$, and Vw.

As the applicant has pointed out, Onozawa does not accomplish any of what it sets out to accomplish if $Vw = 0$. However, the voltage levels of $-Vs2 = 2.5$ V, $Vs1 = 7.5$ V, and $Vw = 5$ V enables the operation of Onozawa as it sets out to accomplish since it provides and meets the requirement for the proper operation of Onozawa such that the high voltage in the reset and address period, $Vs1 + (-Vs2) + Vw = 15$ V is greater than the sustain voltage which is $Vs1 + (-Vs2) = 10$ V.

Since the transistors included in well known electronic structures of the panel display driving circuits must be capable of enduring a high voltage ($Vs1 + (-Vs2) + Vw = 15$ V) with such voltage value assignments ($(-Vs2) = 2.5$ V, $Vs1 = 7.5$ V, and $Vw = 5$ V), it will increase the production cost for the driving circuit, which provides a proper motivation to adopt Onozawa's driving circuitry structure.

Furthermore, Onozawa would perform equally well with the voltage values within proper ranges such as ((-Vs2) = 2.3, 2.4, 2.5, 2.6 V, ... & Vs1 = 6.9, 7.2 7.5, 7.8 V, ..., Vw = 4.6, 4.8, 5.0, 5.2 V, ...).

Therefore, it would have been an obvious design choice to indicate Vw to be a middle voltage between the Vs1 and (-Vs2).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Seokyun Moon whose telephone number is (571) 272-5552. The examiner can normally be reached on Mon - Fri (8:30 a.m. - 5:00 p.m.).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

2005/12/29
Seokyun Moon

Seokyun Moon

SUMATI LEFKOWITZ
SUPERVISORY PATENT EXAMINER